Amendments to the Specification:

Please replace paragraph [0007] with the following amended paragraph.

[0007] Nearly all computer systems now exhibit some aspect of one or more of these types of parallelism. For example, Multimedia extensions (MMX) ~~MMX extensions~~ are SIMD; multiple processors (graphics processors, etc.) are MIMD; pipelining (especially in graphics accelerators) is MISD. Furthermore, techniques such as out-of-order execution and multiple execution units have been used to introduce parallelism within conventional CPUs as well.

Please replace paragraph [0039] with the following amended paragraph.

[0039] In the current embodiment, the Q-registers 34 are operable to merge data into a floating point format and the M-Registers 36 are operable to de-merge data from a floating point format into a single magnitude plus an exponent format. The ALU 32 is a multiplier-adder operable (among others) to receive information from the Q-registers 34 and M-registers 36, execute tasks assigned by the TDU 18 (see FIG. 1), and transmit results to the shift control and condition logic 38 and to the result register pipeline 40. The result register pipeline 40 is operable to communicate with the register file 42, which holds data for transfer into or out of the DRAM modules 22 via a DRAM interface 44. Data is transferred between the PE and the DRAM module 22 via a pair a registers, one register being responsive to the DCU 20 and the other register being responsive to the PE 30. The DRAM interface receives command information from the DCU 20. The DRAM interface 44 also permits the PE 30 to communicate with the host through the host memory access port 48 ~~46~~.

Please replace the Abstract with the following amended abstract:

A method of determining an interleave pattern for n lots of A and y lots of B, when n plus y equals a power of two such that the expression 2^z-n may be used to represent the value of y, includes ~~is comprised of~~ generating a key including ~~comprised of~~ the reverse bit order of a serially indexed count from 0 to 2^z. An interleave pattern can be generated from the key in which all values less than n are replace by A and all other values are replaced by B. In cases where n plus y does not equal a power of two, the method includes ~~is comprised of~~ selecting a value of 2^z where, preferably, $(n + y) < 2^z < 2(n + y)$. A list is created in which the entries include ~~are comprised of~~ the reverse bit order of a serially indexed count from 0 to 2^z. A portion of the list is selected and renumbered to form a key. An interleave pattern can be generated from the key in which all values in the key less than n are replaced by A and all other values in the key are replaced by B. In both cases, the keys can be used to generate a table that contains all possible combinations of values of A and B. The table can then be stored such that an interleave pattern can be automatically selected based on either the number of lots of A or the number of lots of B.